What is claimed is:

1. A flip flop comprising:

a state retention portion to store a bit of digital data, said state retention portion having a first storage node and a second storage node; and

a clocking portion to transfer a new bit of digital data to said state retention portion in response to a clock signal, said clocking portion including:

a first stack of transistors coupled to said first storage node to draw current from said first storage node when a first digital data value is being transferred to said state retention portion, said first stack of transistors including a first transistor having a gate terminal coupled to receive said clock signal and a second transistor having a gate terminal coupled to receive a delayed, inverted version of said clock signal.

2. The flip flop of claim 1, wherein:

said first and second transistors are N-type insulated gate field effect transistors (IGFETs).

3. The flip flop of claim 1, wherein said clocking portion further comprises:

a second stack of transistors coupled to said second storage node to draw current from said second storage node when a second digital data value is being transferred to said state retention portion, said second digital data value being different from said first digital data value, said second stack of transistors including a third transistor having a gate terminal coupled to receive said clock signal and a fourth transistor having a gate terminal coupled to receive a delayed, inverted version of said clock signal.

4. The flip flop of claim 3, wherein:

said third and fourth transistors are N-type insulated gate field effect transistors (IGFETs).

5. The flip flop of claim 3, wherein:

said gate terminal of said first transistor is connected to said gate terminal of said third transistor and said gate terminal of said second transistor is connected to said gate terminal of said fourth transistor.

6. The flip flop of claim 1, wherein said clocking portion comprises:

a clock node to receive said clock signal; and

an inversion device coupled between said clock node and said gate of said second transistor.

7. The flip flop of claim 6, wherein:

said inversion device includes a conventional inverter.

8. The flip flop of claim 6, wherein:

said inversion device includes a NOR gate having first and second input terminals and an output terminal, said first input terminal being connected to said clock node, said output terminal being connected to said gate terminal of said second transistor, and said second input being an enable input of said flip flop.

9. The flip flop of claim 1, wherein:

said state retention portion includes a single latch.

10. The flip flop of claim 9, wherein:

said single latch includes first and second inverters in a cross coupled configuration.

11. The flip flop of claim 10, wherein:

said state retention portion includes a first pull up circuit connected between said first inverter and a power supply node and a second pull up circuit connected

between said second inverter and said power supply node, said first pull up circuit having a first pull up transistor and a second pull up transistor connected in parallel to provide two separate pull up paths for said first inverter.

12. The flip flop of claim 11, wherein:

said first pull up transistor is larger than said second pull up transistor.

13. The flip flop of claim 3, further comprising:

a next state generation portion, connected to said clocking portion, to receive said new bit of digital data from an external source before it is transferred to said state retention portion by said clocking portion.

14. The flip flop of claim 13, wherein:

said next state generation portion includes at least one inversion device to invert a digital signal.

15. The flip flop of claim 14, wherein:

said next state generation portion includes an input node and a first inversion device connected between said input node and an end of said first stack of transistors.

16. A flip flop comprising:

a state retention portion to store a bit of digital data, said state retention portion including:

first and second inverters arranged in a cross-coupled configuration;

a first pull up circuit connected between said first inverter and a power supply node; and

a second pull up circuit connected between said second inverter and said power supply node;

wherein said first pull up circuit includes a first pull up transistor and a second pull up transistor connected in parallel to provide two separate pull up paths for said first inverter.

17. The flip flop of claim 16, wherein:
said first pull up transistor is larger than said second pull up transistor.

18. The flip flop of claim 16, comprising:
a next state generation portion to receive, at an input node thereof, a new bit of digital data to be stored in said state retention portion; and
a clocking portion to transfer said new bit of digital data from said next state generation portion to said state retention portion in response to a clock signal.

19. The flip flop of claim 18, wherein said clocking portion comprises:
a first stack of transistors connected to an input of said first inverter, said first stack of transistors including a first transistor having a gate terminal coupled to receive said clock signal and a second transistor having a gate terminal coupled to receive a delayed, inverted version of said clock signal.

20. The flip flop of claim 19, wherein said clocking portion comprises:
a second stack of transistors connected to an input of said second inverter, said second stack of transistors including a third transistor having a gate terminal coupled to receive said clock signal and a fourth transistor having a gate terminal coupled to receive a delayed, inverted version of said clock signal.

21. The flip flop of claim 18, wherein:
said next state generation portion includes a first inversion device coupled between said input node and an end of said first stack of transistors and a second

inversion device coupled between said end of said first stack of transistors and an end of said second stack of transistors.

22. A method comprising:

providing a memory cell having first and second complementary storage nodes;

providing a first transistor stack coupled to said first storage node of said memory cell, said first transistor stack having first and second transistors;

providing a second transistor stack coupled to said second storage node of said memory cell, said second transistor stack having third and fourth transistors; and

clocking a new data bit to said memory cell, wherein clocking includes:

turning on said first and third transistors at a first instant in time; and

turning off said second and fourth transistors a short period of time after said first instant in time.

23. The method of claim 22, wherein:

clocking a new data bit to said memory cell includes:

applying a clock signal to gate terminals of said first and third transistors; and

applying a delayed, inverted version of said clock signal to gate terminals of said second and fourth transistors.

24. The method of claim 23, wherein:

applying a delayed, inverted version of said clock signal to gate terminals of said second and fourth transistors includes applying said clock signal to an input of an inverter that has an output coupled to said gate terminals of said second and fourth transistors.

25. The method of claim 22, wherein:

applying a delayed, inverted version of said clock signal to gate terminals of said second and fourth transistors includes applying said clock signal to an input of a NOR gate that has an output coupled to said gate terminals of said second and fourth transistors.

26. The method of claim 22, wherein:

providing a memory cell includes providing first and second inverters in a cross coupled configuration, wherein said first complementary storage node includes an input to said first inverter and said second complementary storage node includes an input to said second inverter.

27. A computing system comprising:

a digital processing device having at least one flip flop including:

a state retention portion to store a bit of digital data, said state retention portion having a first storage node and a second storage node, and

a clocking portion to transfer a new bit of digital data to said state retention portion in response to a clock signal, said clocking portion including a first stack of transistors coupled to said first storage node to draw current from said first storage node when a first digital data value is being transferred to said state retention portion, said first stack of transistors including a first transistor having a gate terminal coupled to receive said clock signal and a second transistor having a gate terminal coupled to receive a delayed, inverted version of said clock signal; and

a flash memory coupled to said digital processing device.

28. The computing system of claim 27, wherein:

said clocking portion further comprises a second stack of transistors coupled to said second storage node to draw current from said second storage node when a second

digital data value is being transferred to said state retention portion, said second digital data value being different from said first digital data value, said second stack of transistors including a third transistor having a gate terminal coupled to receive said clock signal and a fourth transistor having a gate terminal coupled to receive a delayed, inverted version of said clock signal.

29. The computing system of claim 27, wherein:

said clocking portion comprises a clock node to receive said clock signal and an inversion device coupled between said clock node and said gate of said second transistor.

30. The computing system of claim 27, wherein:

said state retention portion includes a single latch.